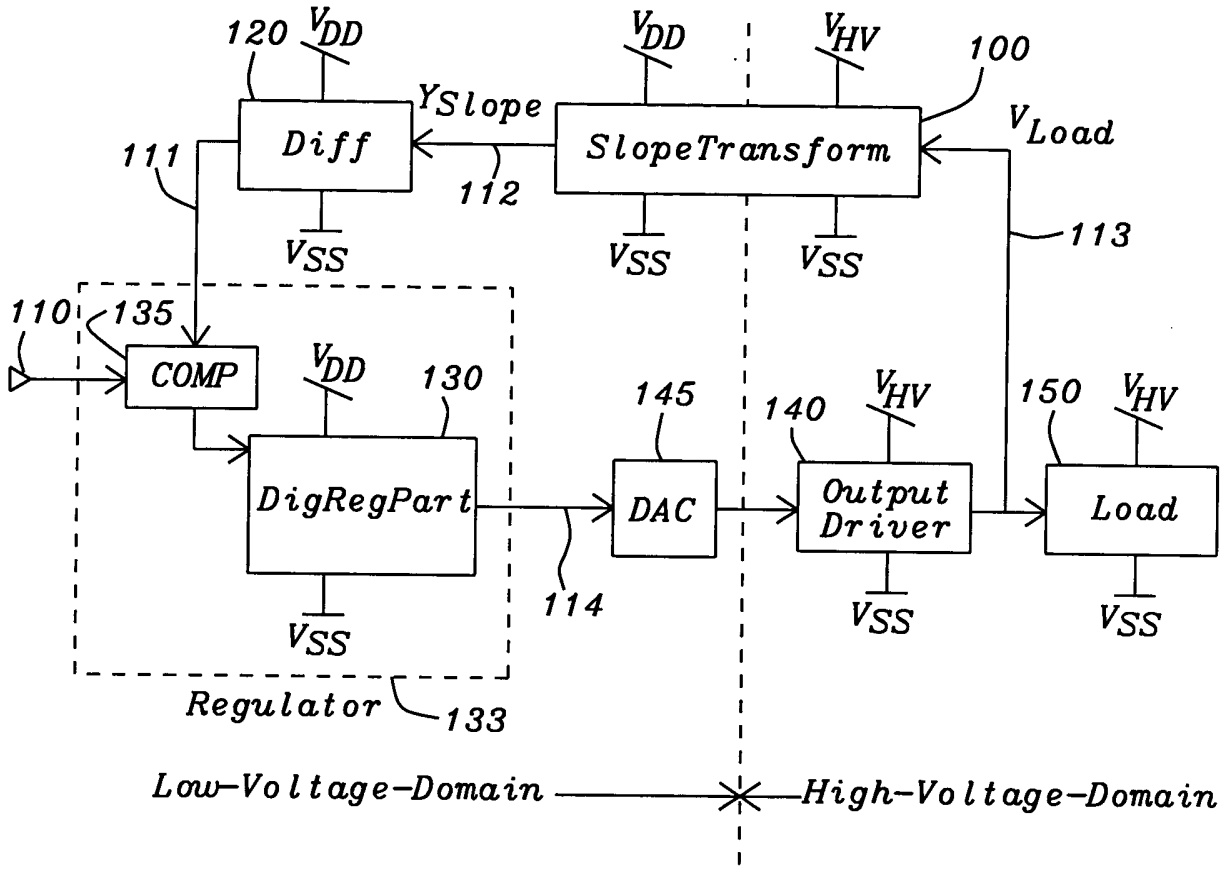
120
V_{DD}
V_{DD}
V_{HV}
100
Diff
YSlope
SlopeTransform
V_{Load}
111
112
113
V_{SS}
V_{SS}
V_{SS}
110
135
COMP
V_{DD}
130
145
140
V_{HV}
150
V_{HV}
DigRegPart
DAC
Output Driver
Load
114
V_{SS}
V_{SS}
V_{SS}
Regulator
133
Low-Voltage-Domain
High-Voltage-Domain

FIG. 1

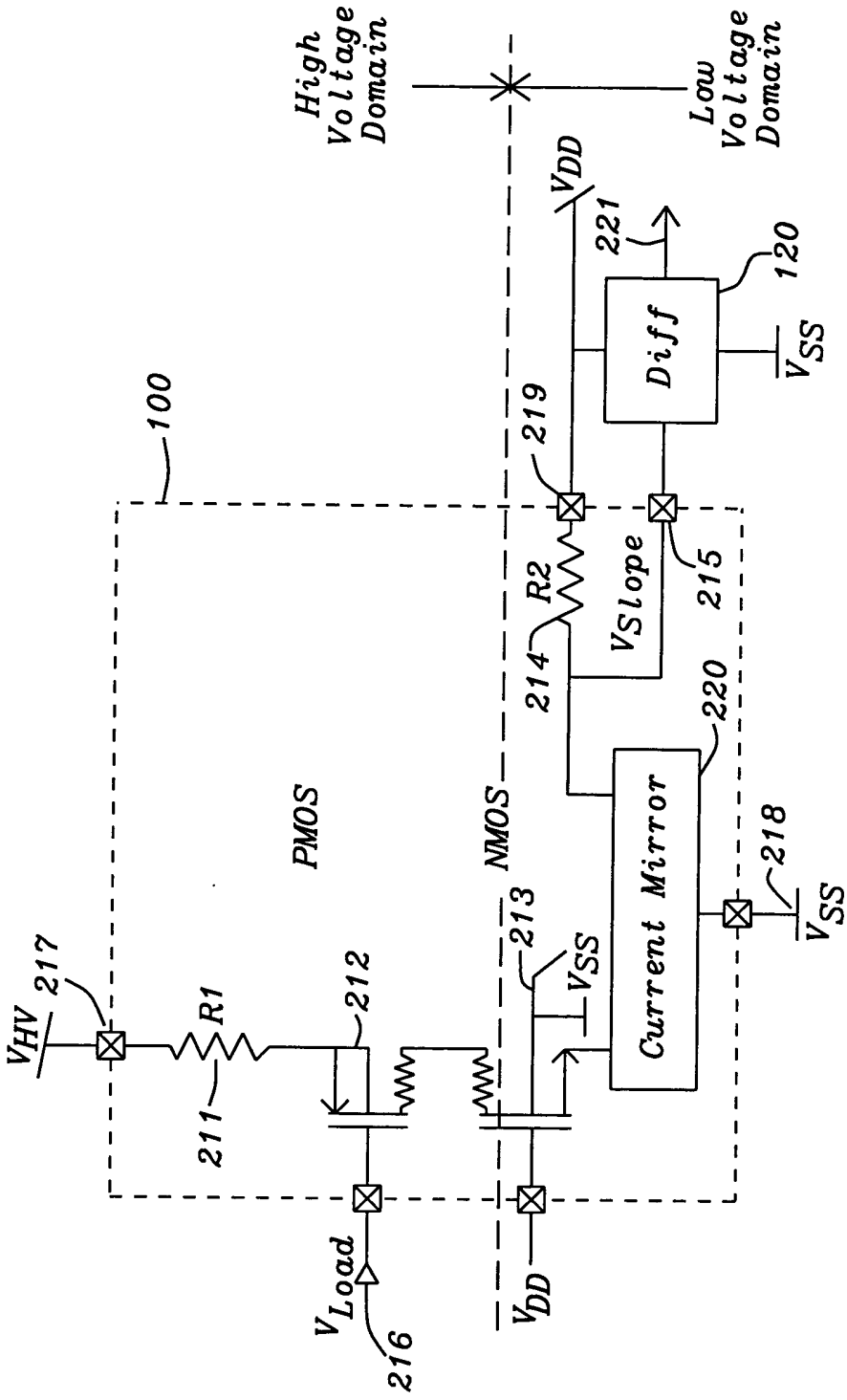
High Voltage Domain
Low Voltage Domain
100
PMOS
NMOS
V_{HV}
217
R1
211
212
213
V_{SS}
Current Mirror
220
218
V_{SS}
V_{Load}
216
V_{DD}
R2
214
V_{Slope}
215
219
V_{DD}
221
Diff
120
V_{SS}

FIG. 2a

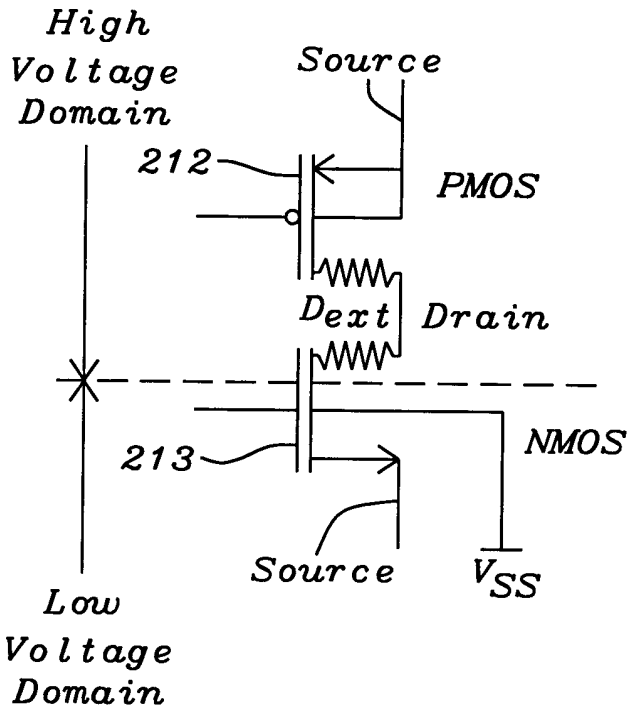
High
Voltage
Domain
Source
212
PMOS
Dext
Drain
213
NMOS
Source
VSS
Low
Voltage
Domain

FIG. 2b

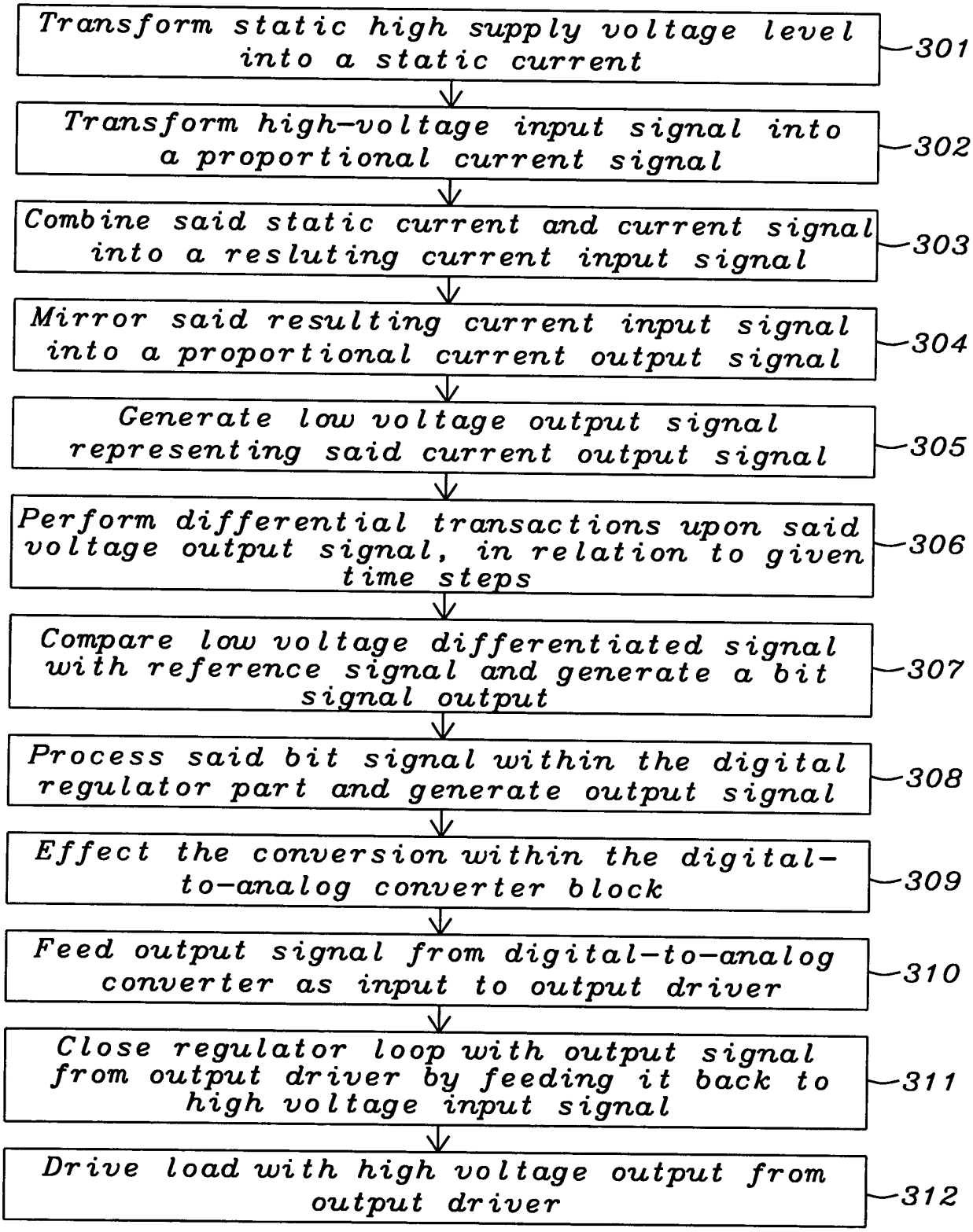
Transform static high supply voltage level into a static current
301
Transform high-voltage input signal into a proportional current signal
302
Combine said static current and current signal into a resluting current input signal
303
Mirror said resulting current input signal into a proportional current output signal
304
Generate low voltage output signal representing said current output signal
305
Perform differential transactions upon said voltage output signal, in relation to given time steps
306
Compare low voltage differentiated signal with reference signal and generate a bit signal output
307
Process said bit signal within the digital regulator part and generate output signal
308
Effect the conversion within the digital-to-analog converter block
309
Feed output signal from digital-to-analog converter as input to output driver
310
Close regulator loop with output signal from output driver by feeding it back to high voltage input signal
311
Drive load with high voltage output from output driver
312

FIG. 3